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Question Paper Code : 77112

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering and Robotics and Automation Engineering)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $Y = A + B\overline{C} + AB + \overline{A}BC$ into canonical form.

2. State the advantages of CMOS logic.

3. Draw the two bit comparator circuit using logic gates.

4. Write down the difference between demultiplexer and decoder.

5. Draw the truth table of RS flipflop.

6. What is the minimum no of flip flop needed to design a counter of modulus 60?

7. What is the basic difference between the RAM & ROM circuitry?

8. Compare a static and dynamic RAM cell.

9. Distinguish between a combinational logic circuit and a sequential logic circuit.

10. What is the most important consideration in making state assignments for asynchronous network?

PART B — (5 × 16 = 80 marks)

11. (a) Simply using Quine Mccluskey method and verify your result using K-map $F = \Sigma(0,1,2,5,7,8,9,10,13,15)$. (16)

Or

(b) (i) Express the Boolean functions $F = A + \overline{B}C$ in a sum of minterms. (10)

(ii) Simplify the following Boolean expression using Boolean algebra.

(1) $\overline{x}\,\overline{y}\,z + \overline{x}\,y\,z + x\,\overline{y}$ (3)

(2) $x\,y\,z + \overline{x}\,z + y\,z$. (3)

12. (a) (i) Design a 4*1 multiplexer circuit. (8)

(ii) Implement the function using multiplexer $F = \Sigma(0,1,3,4,8,9,15)$. (8)

Or

(b) (i) Draw the logic diagram of Binary to octal decoder and explain the working in detail. (8)

(ii) How is the carry look ahead adder faster than a ripple carry adder? Explain in detail with neat sketches. (8)

13. (a) Using D flipflops design a synchronous counter which counts in the sequence. 000, 001, 010, 011, 100, 101, 110, 111, 000. (16)

Or

(b) (i) Discuss the working of a 4 bit Johnson counter with neat block diagram. (8)

(ii) Explain the functioning of a recirculating shift register with various modes of operation. (8)

14. (a) (i) Explain memory decoding. Compare the RAM, ROM, PROM & EPROM. (8)

(ii) Draw a RAM Cell and explain its working in detail. (8)

Or

(b) Write short notes on with suitable schematic (16)

(i) Programmable Logic Array (PLA).

(ii) Field Programmable Gate Arrays (FPGA).

15. (a) (i) Explain how a state graph for a sequential machine can be convened to an equivalent ASM chart. (8)

(ii) Derive the ASM chart for binary multiplier. (8)

Or

(b) (i) When is a sequential machine said to be strongly connected. (2)

(ii) Design a sequential pattern detector that receives a stream of input bits. The circuit should recognize the pattern 010 and produce an output whenever this pattern is received. (14)

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